

55. A method as recited in claim 54, wherein forming the test structures comprises forming a first layer portion from a first conductive layer and forming a first via within a first insulating layer, the method further comprising coupling the first layer portion to the at least one dummy filling through the first via.

56. A method as recited in claim 55, wherein forming the test structures further comprises forming a second via in a second insulating layer and coupling the first layer portion to a substrate of the semiconductor die through the second via.

57. A method as recited in claim 56, wherein the first or second via is a redundant via.

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58. A method as recited in claim 56, further comprising performing voltage contrast testing on the dummy fillings to detect a defect, wherein a defect is detected when the at least one dummy filling coupled to the test structure does not have a voltage potential that differs from a voltage potential of the other non-coupled dummy fillings.

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59. A method as recited in claim 56, wherein forming the test structure comprises forming a plurality of conductive layer portions and vias within a plurality of insulating layers, the vias being interleaved between the plurality of conductive layers to form a multilevel test structure.

60. A method as recited in claim 59, wherein at least one of the vias is a redundant via.

61. A method of forming a test pattern on a semiconductor die, comprising:

a. forming a first plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_1 , (2) each of the metal lines has a width of W_1 , and (3) the metal lines are alternately electrically isolated; and

b. forming a second plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_2 , (2) each of the metal lines has a width of W_2 , (3) the metal lines are alternately electrically isolated, and (4) W_1 does not equal W_2 .

62. The method of claim 61, wherein each of the metal lines in the first and second pluralities of substantially parallel metal lines have substantially the same length.

63. The method of claim 62, wherein the length of each of the metal lines in the first and second pluralities of substantially parallel metal lines does not exceed 10 microns.

64. The method of claim 63, wherein the length of each of the metal lines in the first and second pluralities of substantially parallel metal lines does not exceed 5 microns.

65. The method of claim 63, wherein W_1 and W_2 do not exceed 2.5 microns.

66. The method of claim 64, wherein W_1 and W_2 do not exceed 1.25 microns.

67. The method of claim 61, further comprising forming a third plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_3 , (2) each of the metal lines has a width of W_3 , (3) the metal lines are alternately electrically isolated, and (4) W_3 does not equal W_1 or W_2 .

68. The method of claim 61, wherein the metal lines in the first and second pluralities of substantially parallel metal lines are all of the substantially same length.

69. The method of claim 61, wherein the first plurality of substantially parallel lines and the second plurality of substantially parallel lines each covers substantially the same amount of area on the semiconductor die.

70. The method of claim 61, wherein the first plurality of substantially parallel lines comprises more metal lines than does the second plurality of substantially parallel lines.

71. A method of fabricating a test pattern on a semiconductor die, comprising:

forming an electrically-isolated metal line; and

forming a non-electrically-isolated metal line, wherein both the lines have the same width, are substantially parallel to each other and are spaced apart by their width.

72. The method of claim 71, wherein the metal lines have substantially the same length.

73. The method of claim 72, wherein the length of each of the metal lines does not exceed 10 microns.

74. The method of claim 73, wherein the length of each of the metal lines does not exceed 5 microns.

75. The method of claim 73, wherein the width of the lines does not exceed 2.5 microns.

76. The method of claim 74, wherein the width of the lines does not exceed 1.25 microns.

77. A method of fabricating a test structure for detecting defects in a semiconductor die caused by chemical mechanical polishing, the method comprising:

forming a first metal line disposed on a semiconductor die, the first metal line having a length L and width W_1 and extending in a first direction;

forming a second metal line disposed on a semiconductor die adjacent to the first line, the second metal line having a length L_1 and width W_1 and extending in a first direction;

forming a third metal line disposed on the semiconductor die adjacent to the second metal line, the third metal line having a length L_2 and width W_2 and extending in the first direction; and

forming a fourth metal line disposed on the semiconductor die adjacent to the third metal line, the fourth metal line having a length L_2 and width W_2 and extending in the first direction,

wherein L_1 and L_2 are not equal and the first, second, third, and fourth metal lines are alternately electrically isolated.

78. The method of claim 77, wherein W_1 and W_2 are not equal.

79. The method of claim 77, further comprising:

forming a fifth metal line disposed on the semiconductor die adjacent to the fourth metal line, the fourth metal line having a length L_3 and width W_3 and extending in the first direction; and

forming a sixth metal line disposed on the semiconductor die adjacent to the fifth metal line, the fifth metal line having a length L_3 and width W_3 and extending in the first direction,

wherein L_3 is not equal to L_1 or L_2 and the fourth, fifth, and sixth metal lines are alternately electrically isolated.

80. The method of claim 79, wherein W_3 is not equal to W_1 or W_2 .

81. The method of claim 77, wherein each of L_1 and L_2 is less than 10 microns.

82. The method of claim 80, wherein W_1 is greater than W_2 , and W_2 is greater than W_3 .

83. The method of claim 77, wherein those metal lines that are not electrically isolated are connected to ground.

84. The method of claim 80, wherein each of L_1 , L_2 , and L_3 is less than 20 microns and each of W_1 , W_2 , and W_3 is less than 5 microns.

85. The method of claim 84, wherein each of L_1 , L_2 , and L_3 is less than 10 microns and each of W_1 , W_2 , and W_3 is less than 2 microns.

86. A method of fabricating a plurality of metal test structures on a semiconductor die, the method comprising:

- a. forming a first section having a first plurality of test structures, wherein the test structures of the first plurality of test structures each has the same horizontal aspect ratio; and
- b. forming a second section having a second plurality of test structures, wherein the test structures of the second plurality of test structures each has the same horizontal aspect ratio but has a horizontal aspect ratio different than the horizontal aspect ratio of the first plurality of test structures.

87. A method of fabricating a test pattern on semiconductor die, the method comprising:

a. forming a first plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_1 , (2) each of the metal lines has a width of W_2 , (3) the metal lines are alternately electrically isolated, and (4) the sum of W_1 and W_2 is a constant K ; and

b. forming a second plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_3 , (2) each of the metal lines has a width of W_4 , (3) the metal lines are alternately electrically isolated, (4) W_1 does not equal W_3 , and (5) the sum of W_3 and W_4 equals the constant K .

88. The method of claim 87, wherein each of the metal lines in the first and second pluralities of substantially parallel metal lines have substantially the same length.

89. The method of claim 88, wherein the length of each of the metal lines in the first and second pluralities of substantially parallel metal lines does not exceed 10 microns.

90. The method of claim 89, wherein the length of each of the metal lines in the first and second pluralities of substantially parallel metal lines does not exceed 5 microns.

91. The method of claim 87, wherein W_1 and W_3 do not exceed 2.5 microns.

92. The method of claim 87, wherein W_1 and W_3 do not exceed 1.25 microns.

93. The method of claim 87, further comprising forming a third plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_5 , (2) each of the metal lines has a width of W_6 , (3) the metal lines are alternately electrically isolated, (4) W_5 does not equal W_1 or W_3 and (5) the sum of W_5 and W_6 equals the constant K .

94. The method of claim 93, wherein the metal lines in the first, second and third pluralities of substantially parallel metal lines are all of the substantially same length.

95. The method of claim 87, wherein the first plurality of substantially parallel lines and the second plurality of substantially parallel lines each covers substantially the same amount of area on the semiconductor die.

96. The method of claim 87, wherein the first, second and third plurality of substantially parallel lines each comprise the same number of lines.

97. A method of fabricating a semiconductor device, the method comprising:

forming a first plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_1 , (2) each of the metal lines has a width of W_2 , (3) the metal lines are alternately electrically isolated, and (4) the sum of W_1 and W_2 is a constant K ; and

forming a second plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_3 , (2) each of the metal lines has a width of W_4 , (3) the metal lines are alternately electrically isolated, (4) W_1 does not equal W_3 , and (5) the sum of W_3 and W_4 equals the constant K .

98. The method of claim 97, wherein each of the metal lines in the first and second pluralities of substantially parallel metal lines have substantially the same length.

99. The method of claim 98, wherein the length of each of the metal lines in the first and second pluralities of substantially parallel metal lines does not exceed 10 microns.

100. The method of claim 99, wherein the length of each of the metal lines in the first and second pluralities of substantially parallel metal lines does not exceed 5 microns.

101. The method of claim 97, wherein W_1 and W_3 do not exceed 2.5 microns.

102. The method of claim 97, wherein W_1 and W_3 do not exceed 1.25 microns.

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103. The method of claim 97, further comprising forming a third plurality of substantially parallel metal lines, wherein (1) the metal lines are spaced apart by spaces of width W_5 , (2) each of the metal lines has a width of W_6 , (3) the metal lines are alternately electrically isolated, (4) W_5 does not equal W_1 or W_3 and (5) the sum of W_5 and W_6 equals the constant K .

104. The method of claim 103, wherein the metal lines in the first, second and third pluralities of substantially parallel metal lines are all of the substantially same length.

105. The method of claim 97, wherein the first plurality of substantially parallel lines and the second plurality of substantially parallel lines each covers substantially the same amount of area on the semiconductor die.

106. The method of claim 97, wherein the first, second and third plurality of substantially parallel lines each comprise the same number of lines.